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Implementation of Full duplex communication using Serial Peripheral interface communication protocol

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ABSTRACT

Alongside advancements of VLSI advances, the whole mechanical control PC framework can be incorporated into one chip called modern control System on Chip. The devices can be controlled using the different data transferring protocols; viz. SPI (serial Peripheral Interface), Ethernet, UART etc. The paper discusses about implementation of the Serial Peripheral Interface. The serial and parallel interface assumes a vital part in correspondence between modern control framework and the peripherals. The paper discusses implementation of the SPI protocol in between two microcontrollers. One of the microcontroller acts as the master and another one acts as slave. Master sends the data through bus and slave receives the data and gives the acknowledgement and also sends the data.

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I. INTRODUCTION

Since we are entering into era of atomization. This can be accomplished by applying different advances in different exercises. With a specific end goal to finish errands we have to consider interdisciplinary approach. For the most part in industry diverse conventions are utilized for transmitting information along various microcontrollers and distinctive controlling gadgets. Some of them are SPI: - serial Fringe interface, I2C:- Between incorporated Circuit etc. But keeping in mind the end goal to convey between two unique sorts of gadget which are tolerating two distinct conventions we have to utilize the Serial Peripheral Interface protocol. Since the protocol uses the four data line to transfer the data in between the devices. The data communication is trustable. The loss of the data is minimum as compared to other protocols. The master begins the communication by sending or assigning the clock frequency supported by both the devices. The other device which is acting as slave is selected by the master itself only by assigning the logic level 0 to the select line. And the data transfer takes place on the reaming two data lines. The two microcontrollers or devices will communicated with each other using these two data lines and one clock line and one slave select line. During complete execution of the protocol it makes use of the four line lines which are unidirectional for data and clock whereas the most important is the slave select line.

II. LITERATURE REVIEW

Aviraj Ghanekar, Braj Kishor, Sachin Bandewar have been employed on “Design and then Execution of SPI Bus Protocol” where in here work targets the overall performance evaluation of SPI also with the RTL Model work . Model portion includes around Motorola 3 .0 Specification and so codes develop in the Verilog. Serial peripheral interface RTL split up into 2 blocks one is Master and other is Slave. RTL code compiled all blocks work completed making use of XILINX ISE tool which provides simulation and synthesis validation of specification. [1]
Ndubuisi Ekekwea, Ralph Etienne-Cummingsa, Peter Kazanzides were working on “ A wider full speed range and so higher accuracy positioning and velocity body measurements chip with serial peripheral interface ” through this paper , an incremental encoder-based position and speed measurements VLSI chip with SPI interface have been identified . It is depending on 2 methods: counting pulses from a clock between succeeding pulses of the encoder for low-speed application and counting the numbers of pulses

from the encoder in a best-known time for medium and high data transfer speeds. The combined methods allow the chip to provide higher accuracy for a wide speed range stressed on the supervisory microcontroller. The chip is so compact with low power usage when compared with FPGA versions. It is executed in a 2P3M 0 .5 mm CMOS process. Though designed for utilize in the control unit of a surgical medical robot, maybe used in varieties of testing applications requiring precise motion estimation and control.[2]

Fareha Naqvi has implemented on "Design and Implementation of Serial Peripheral Interface Protocol Using Verilog HDL " in this paper SPI Master and Slave has been implemented using verilog HDL and Xilinx ISE 13.3.1 was used for simulation. The basis of this paper is the focus on data transmission between master and slave modules. They have verified the data in slave device same as the data in the master device and various possible cases of clock polarity and clock phase are verified.[3]

M. Sandya, K. Rajasekhar, have worked on "Design and Verification of Serial Peripheral Interface". In this paper they have designed the SPI Master-Slave core based upon design-reuse methodology. SPI transmission timing is very strict, so in this paper design a reliable and stable clock generation module, both the case of odd-even frequently were considered. Data transmission module is a simple and the transfer speed is faster. They have also done code coverage and achieved Design coverage of 100 percent, and verified the data in slave device same as the data in the master device also done functional verification. The complete function of the registers is done in this paper. The innovation of this article: System verilog language is used in order to cover all the functions of the code.[4]

Varun, Ritula Thakur have assessed on "A Review on PROFINET Fieldbus System" through this article they already have described the most beneficial advantages of fieldbus system.

a) Even more Stress is placed in PROFINET fieldbus adoption in manufacturing domain made due to no adding up equipment requirement of creating communicating link in various industrialized management structural design.
b) In Real time control models, the delay and thus jitter difficulties which are in μs range is defined under Isochronous Real Time category.
c) Non time crucial control models are place in quite hard real time category at which delay and jitter problems are not even more prompting.[5]

Henning Trsek, Juergen Jasperneite, Gunnar Lessmann were employed on "A Concept for the system integration of Wireless Sensor Networks to Industrial Automation System using PROFINET" within this here concept makes use of PROFINET IO as a proper integration instrument, that has also been proved by the ongoing fieldbus integration, and an application level suggestion of the SP100 by way of example for the WSN. The very few readily available remote application level for commercialized automation are of course problems that is a necessity to extend their needs. With the design documented in this paper, it is possible to plan all of the functionalities of the WSN completely on PROFINET I/O with an immediate visibility. This can be accomplished by having the record data read/write operations from PROFINET along with corresponding slot/subslot addressing. More than that, the attained adaptability of the wireless physical level can only be of a restricted advantage, because of the readily available engineering paradigm of commercial enterprise automation.[6]

P. Ferrari, A. Flammini, D. Marioli, A. Taroni were employed on "Experimental evaluation of PROFINET performance" within this paper the utilization Industrialized Ethernet in a real-time environmental conditions is found to be the upcoming of distributed automation. PROFINET could be defined as an ideal ways to understand RTE network: its support to difficult real-time makes it possible latest high-performance motion control application. Integration with existed software tools and the system, for example PROFIBUS slice and OPC SCADA have been absolutely calculated. Preparatory experiential the results explain a very excellent timing patterns of the RT protocol , with cycle time period down to I/O ms (suitable for average field device) and variability no more than 10%.[7]

III. BLOCK DIAGRAM

The main components of this proposed system are ARM7 LPC2148 microcontroller, LCD (liquid crystal display), PLC (programmable logical device) and microcontroller assembly interacting with each other as shown in block diagram.

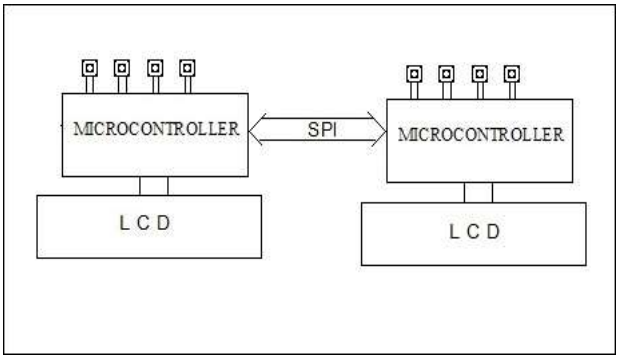

Fig.1: Basic block diagram

The above block diagram gives the idea about complete full duplex communication taking place in between the two microcontroller. The left side microcontroller is acting as master and on the right side microcontroller is acting as slave and full duplex communication is taking place in between this two different microcontroller systems. The master assigns the frequency to clock pin or serial clock line. This clock line is used for synchronising the complete transmission in between the master and slave. After pressing the button from master side the data transmission begins and the on the other side slave is having the buttons on which indicate the status. This status is then transferred to the master from slave side as acknowledgement.

The both systems are having independent liquid crystal displays which indicate the incoming data from either side and the sending data.

IV. WORKING

Working of the SPI:-

For successful transmission of the data by using serial peripheral interface which is also synchronous data transmission protocol the different data lines are required. There are four data lines which are very important

SCKL, MOSI, MISO, SS.

SCLK: - Serial clock

MOSI: - Master out slave in

MISO: - Master in slave out

SS: - Slave select

The master is very important. The complete data transmission depends on the frequency assigned by master itself. The master assigns the frequency which decides the data transmission rate. The master assigns the frequency which is responsible for data transmission which is assigned to SCK serial clock which is also supported by slave. The master selects the slave device by assigning with logic 0 to select line and waits till the slave is selected.

During each cycle of the clock which is assigned to synchronous clock by the master the full duplex communication occurs. The master transfers the data on the transfer buffer which is acting as shift register which is present in master itself. This is one of the dedicated buffer which are present in microcontroller and designed to work for serial peripheral interface protocol. This transferred data is then further send to the Master out slave in data line which is unidirectional data line. Once the data is reached to the slave side it first enterers in to the data buffer which is acting as shift register having at the slave side. This is also one of the data buffer which are present in microcontroller and designed to work for serial peripheral interface protocol in salve itself. The data is then completely recovered or transfer from this transfer buffer which is shift register for further application. On the other hand slave clears the buffer and again fills the data into the buffer which is again shifting register currently empty with data which is send as reaction or acknowledgement to the master. Then this data is transferred from this data buffer to Master in slave out which is then reaches to the master side using this line and it is then transferred or store at master side in the data buffer which is cleared after transmission of the master out slave in. and again the data is take or transferred from this buffer to the further action. This how the serial peripheral interface protocol is completed. The following diagram shows the complete data lines including other two lines also which are required or used in serial peripheral interface.

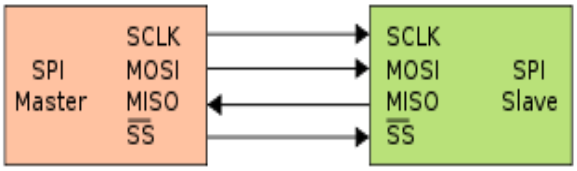

Fig.2: Serial peripheral interface model

V. ALGORITHM

Initially the microcontroller which is acting as master will send the data and will receive the acknowledgement and the slave will select the data and will send the data from transfer buffer and microcontroller will receive the data in receive buffer of microcontroller. And on every step the buffer will be checked and data will be transfer accordingly. And if buffer is full then microcontroller and slave both will wait and then again try to communicate.

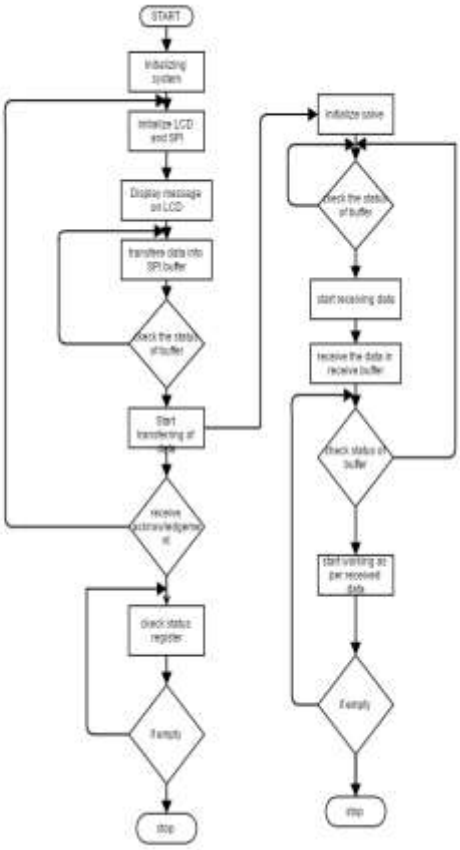

Fig.3: Flow chart

VI. SOFTWARE SIMULATION RESULT

The following diagram shows the simulation of the SPI protocol.

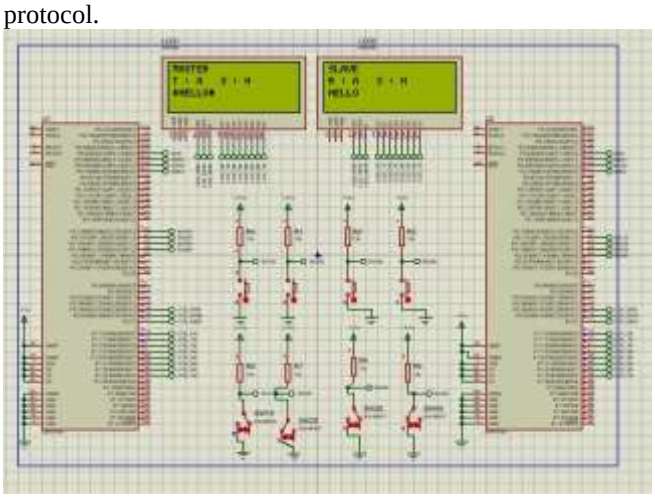

Fig.4: Simulation Results

Explanation of simulation:

The above simulation diagram shows the working of full duplex communication between the two microcontrollers. As mentioned above both the systems are having Advanced RISC Machine 7(LPC2148) microcontrollers, and independent liquid crystal displays. The microcontroller on right side is acting as master and on the other side is acting as slave. Both systems are showing the outputs of successful full duplex communication results on liquid crystal displays. As stated earlier the master and slave both are having buttons which are responsible for the complete communication which is in the form of data transfer. The buttons on microcontroller initiates the data transfer and button on slave side completes with sending the status.

VII.CONCLUSION

Therefore from above simulation results we can see that full-duplex communication is possible in between two microcontrollers. Also we can connect the any form of automation module on the salve or master side with help of any external hardware.

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